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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/183,389	10/29/1998	VLADIMIR BEREZIN	08305/048001	3070

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EXAMINER
WHIPKEY, JASON T

ART UNIT	PAPER NUMBER
2612	19

DATE MAILED: 09/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/183,389	BEREZIN, VLADIMIR	
	Examiner	Art Unit	
	Jason T. Whipkey	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 1998* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 18, 2003, has been entered.

Response to Arguments

2. Since claims 1-8 have been cancelled, Applicant's arguments are rendered moot. Rejections of new claims 9-21 follow.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 9, 15, 18, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Merrill (U.S. Patent No. 5,892,541).

Regarding claim 9, Merrill shows an imaging system 100 in Figure 2 with an array of active pixel sensor cells 110 (column 4, lines 43-53). Detection circuits DC1-DCm (an "analog to digital converter") digitize integration voltages placed on cell output lines CO1-COm by pixel cells 110 (column 7, lines 27-29). The digitized voltages are then output to memory unit 112 ("a digital memory unit") (column 7, lines 27-31). The process repeats, as pixel cells 110 are read multiple times during each integration cycle (column 6, lines 53-62, and column 8, lines 23-27). Voltages may be stored in memory unit 112 as a total accumulation for each pixel cell 110 or as individual partial integration values (column 8, lines 51-54).

Regarding claim 15, Merrill shows in Figure 2 that each column line CO1-COm is connected to one of the detection circuits DC1-DCm (column 4, lines 62-67).

Regarding claim 18, Merrill shows an imaging system 100 in Figure 2 with an array of active pixel sensor cells 110 (column 4, lines 43-53). As shown in Figure 7, cell 110 is implemented as cell 200 and is formed on substrate 210 (column 11, lines 40-46). Detection circuits DC1-DCm digitize integration voltages placed on cell output lines CO1-COm by pixel cells 110 (column 7, lines 27-29). The digitized voltages are then output to memory unit 112 ("a digital memory") (column 7, lines 27-31). The process repeats, as pixel cells 110 are read multiple times during each integration cycle (column

6, lines 53-62, and column 8, lines 23-27). Voltages may be stored in memory unit 112 as a total accumulation for each pixel cell 110 or as individual partial integration values (column 8, lines 51-54).

Regarding claim 20, Merrill teaches that unit 112 outputs a total pixel output voltage for each cell after the entire integration period is complete (column 9, lines 29-35).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merrill (U.S. Patent No. 5,892,541) in view of Lee (U.S. Patent No. 6,583,817).

Claims 10 and 19 may be treated like claims 9 and 18, respectively. While Merrill shows a prior-art CMOS active pixel sensor cell 10 in Figure 1 (column 1, lines 34-40), Merrill is silent with regard to cell 110 being fabricated in CMOS.

Lee discloses an active pixel sensor (Figure 6a) fabricated in CMOS. As stated in column 1, lines 20-35, advantages to fabricating active pixel sensors in CMOS include low voltage operation and low power consumption, process compatibility with

on-chip electronics, and potentially lower cost as compared to the conventional CCD, because of the wide availability of the standard CMOS manufacturing process. For these reasons, it would have been obvious at the time of invention for Merrill to fabricate his pixel cells in CMOS.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Merrill (U.S. Patent No. 5,892,541) in view of Mandl (U.S. Patent No. 5,248,971).

Claim 11 may be treated like claim 9. However, Merrill is silent with regard to detection circuits DC1-DCm being an oversampling converter.

Mandl shows in Figures 3A and 3B a video camera that uses an oversampling A/D converter (column 4, line 67 through column 5, line 3). A/D converter 144 in Figure 3B digitizes charges from array column 156 (column 5, line 67 through column 6, line 16). The charges from array column 156 are oversampled (column 6, lines 50-56).

As stated in column 10, lines 14-20, an oversampling A/D converter in an imaging system improves image quality. For this reason, it would have been obvious to have Merrill's system utilize an oversampling A/D converter.

8. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merrill (U.S. Patent No. 5,892,541) in view of Lee (U.S. Patent No. 6,466,265).

Claim 12 may be treated like claim 9. However, Merrill is silent with regard to including an analog signal processor including analog double sampling circuitry.

Lee discloses an active pixel sensor, as shown in Figure 2e. Pixel data is sent via each column bus to a correlated double sampling circuit 91 (column 4, lines 24-27).

An advantage to performing double sampling on an image signal is that noise is reduced, resulting in an image of better quality. For this reason, it would have been obvious at the time of invention for Merrill to include double sampling circuitry in his image sensor.

Regarding claim 13, Lee teaches that the double sampling circuitry receives a reset sample ("a reference") and a signal sample from an active pixel (column 5, lines 36-43). It is inherent that correlated double sampling circuitry decreases fixed pattern noise.

Regarding claim 14, Lee shows in Figure 4 that the analog processing performed on the column pixel signals includes amplification by programmable gain amplifier 93 (column 5, lines 23-35). Programmable gain amplifier may use a variable gain element (column 5, lines 52-54).

An advantage to using a variable gain amplifier is that the gain of the pixel signals may be adjusted to reach a uniform value based on lighting conditions. For this reason, it would have been obvious at the time of invention to have Merrill's image sensor include a variable gain amplifier.

9. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merrill (U.S. Patent No. 5,892,541).

Claim 16 may be treated like claim 9. However, Merrill is silent with regard to including a digital signal processor between detection circuits DC1-DCm and memory unit 112.

Official Notice is taken that digital signal processing is commonly performed on pixel data before it is stored in memory. An advantage to performing DSP is that image quality may be improved.

For this reason, it would have been obvious at the time of invention to have Merrill include a digital signal processor between detection circuits DC1-DCm and memory unit 112.

Regarding claim 17, Merrill teaches that unit 112 outputs a total pixel output voltage for each cell after the entire integration period is complete (column 9, lines 29-35).

10. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Merrill (U.S. Patent No. 5,892,541) in view of Fossum (U.S. Patent No. 5,665,959).

Merrill shows an imaging system 100 in Figure 2 with an array of active pixel sensor cells 110 (column 4, lines 43-53). Detection circuits DC1-DCm (an "analog to digital converter") digitize integration voltages placed on cell output lines CO1-COm by pixel cells 110 (column 7, lines 27-29). The digitized voltages are then output to memory unit 112 ("a digital memory array") (column 7, lines 27-31). The process repeats, as pixel cells 110 are read multiple times during each integration cycle (column 6, lines 53-62, and column 8, lines 23-27). Voltages may be stored in memory unit 112

as a total accumulation for each pixel cell 110 or as individual partial integration values (column 8, lines 51-54).

Merrill is silent with regard to the components being on a substrate.

Fossum discloses a focal plane array 12 with CMOS pixels (column 6, lines 15-18) and a buffer memory 23, shown in Figure 7. The system shown in Figure 7 may be monolithic (column 9, lines 52-54).

As stated in column 9, lines 63-65, the advantage to using a monolithic architecture is that performance is increased, in contrast with a system that uses separate components. For this reason, it would be obvious to have Merrill's system formed on a single substrate.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason T. Whipkey, whose telephone number is (703) 305-1819. The examiner can normally be reached Monday through Friday from 9 A.M. to 6:30 P.M. eastern daylight time, alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R. Garber, can be reached on (703) 305-4929. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communication and (703) 872-9315 for After Final communication.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, whose telephone number is (703) 306-0377.

Response to this action should be mailed to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to the appropriate number above for communications intended for entry. (For informal or draft communications, please label **"PROPOSED"** or **"DRAFT"**.) Hand-delivered responses should be brought to the sixth floor receptionist of Crystal Park II, 2121 Crystal Drive in Arlington, Virginia.

JTW
JTW
September 10, 2003

VU LE
PRIMARY EXAMINER